The BaBar Silicon Vertex Tracker

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Abstract

The BaBar Silicon Vertex Tracker is a five-layer, double-sided silicon-strip detector designed to perform vertex measurements of B decays at the PEP-II asymmetric e^+e^- collider. I discuss the main detector design considerations and features, as well as preliminary measurements of the combined noise of the detector and its readout system.

1 Physics Goals, Design Issues, and Accelerator Constraints

The primary goal of the BaBar experiment [1] is to measure CP-violating asymmetries in the neutral B meson system. The experiment will use the PEP-II e^+e^- storage ring at the Stanford Linear Accelerator Center (SLAC), which has a design luminosity of $\mathcal{L} = 3.0 \times 10^{33}$ cm^{-2}s^{-1}, giving 15 M $B^0\bar{B}^0/10^7$ s. The most important feature of PEP-II, apart from its high luminosity, is the asymmetry in beam energies, $E_{e^-} = 9.000$ GeV and $E_{e^+} = 3.109$ GeV. The CM energy is equal to the mass of the $\Upsilon(4S)$, but the unequal beam energies give the $\Upsilon(4S)$ a boost $\beta\gamma = 0.56$ along the beam (z) direction. As a consequence, the B^0 and $\bar{B}^0$ mesons produced in the $\Upsilon(4S)$ decay have a mean separation $\Delta z \approx 260$ μm for $\tau_{B^0} = 1.55$ ps. It is crucial that this separation is large enough to be measured, since it allows CP asymmetries to be studied as a function of the time difference $t = t_{\rm CP} - t_{\rm tag} \approx \Delta z/\beta\gamma$ between the decay of one B meson to a CP eigenstate and the other B meson to a flavor-tagging final state. Because the *time-integrated* CP asymmetry is zero at the $\Upsilon(4S)$, the Silicon Vertex Tracker (SVT) is not merely added to enhance the experiment: it is essential to the main goal of studying CP-violating processes.

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This paper describes the main design considerations and features of the SVT, and it presents preliminary noise results obtained when the detectors were first read out with the new AToM readout ICs. The BaBar SVT has also been described in other recent publications [2,3], and the AToM IC is discussed in a separate paper contributed to this conference [4].

The design of the BaBar SVT is constrained to an unusual degree by the combination of requirements from the CP asymmetry measurements and the demands of the accelerator environment. The most important performance requirements for the SVT are determined from the following considerations:

- The resolution on Δz must be good enough to perform the CP asymmetry measurement. In low background modes, such as $B^0 \to J/\psi K_s^0$, a resolution $\sigma_{\Delta z} = 0.5\langle\Delta z\rangle \approx 130$ μm yields nearly as good a measurement of the CP asymmetry as perfect Δz resolution. (In modes that are less clean, Δz cuts are useful in suppressing backgound, so better resolution is not wasted.) Monte Carlo studies show that, for our detector design, the z resolution on the CP-eigenstate B vertex is typically $\sigma_z \approx 40$ μm, while the resolution on the tagging decay vertex is larger, 60 μm to 80 μm; together, these provide adequate resolution on Δz.
- Due to the boost, the forward hemisphere in the $\Upsilon(4S)$ frame is compressed into the region $\theta \leq 61^\circ$ in the lab frame, where θ is the polar angle to the beam axis. Acceptance in the forward region is therefore extremely important.
- The SVT must have robust pattern recognition, which is one of the considerations that led to a five-layer design. The expected nominal occupancies in the inner layer are between 0.4% and 3.1% (depending on azimuthal angle about the beam axis); these occupancies are dominated by showers due to lost beam particles.
- The expected yearly radiation dose in the SVT inner layer is 33 krad (ϕ averaged); the detector is designed to operate for 10 years at this level.
- The beam bunches cross at the interaction point at $f = 238$ MHz (4.2 ns), which implies that the readout IC must simultaneously acquire, process, and transmit data.

The PEP-II interaction region has a major effect on the SVT design. The electron and positron beams each comprise 1658 bunches, which must be separated before their first parasitic crossing, at about 62 cm from the IP. Permanent dipole magnets (B1), which start at $z \approx \pm 20$ cm, accomplish this task, but they effectively restrict the SVT acceptance in the lab to the region $\theta \geq 350$ mr to the beam axis. The SVT is mounted on 1-mm-thick carbon-fiber cones (Fig. 1) supported by the B1 magnets; the region within 1 cm of the cone outer surface is used for SVT readout electronics and cabling, which are outside of the tracking volume.

2 Detector Description

The BaBar SVT consists of five layers, as shown in Fig. 1 and Fig. 2. The beampipe is a double-walled, water-cooled Be structure with 1.06% X_0. The three inner layers, which dominate the vertex measurement, are at radii 32 mm, 40 mm, and 54 mm; each of these layers has six azimuthal modules that are mounted to brass cooling rings on the support cones. Figure 2 shows that the support ribs are glued to the outer surface of the detectors in each layer. Layer 1 detectors are mounted differently from those in other layers in that their support ribs are glued to the inner side of layer 2; these two inner layers thus form a rigid system. Modules in layers 1 and 2 each have four silicon wafers mounted along the z (beam) direction, while those in layer 3 have six wafers. The two outer layers of the SVT are each divided into two sublayers, (4a, 4b) and (5a, 5b), which are at radii (124 mm, 127 mm) and (140 mm, 144 mm). These layers are important for pattern recognition, track linking, and measurement of very low momentum tracks, for example, from $D^* \to D\pi$ decay. To reduce the angle of incidence of forward-going tracks, the end wafers in the outer layers are tilted by 28° (L4) and 24° (L5). Each sublayer in layer 4 contains eight azimuthal modules, while those in layer 5 contain nine modules. Layer 4 modules have 7 silicon detectors along the beam direction, while layer 5 modules have 8.

The tight constraints on detector geometry led to a design using six different types of silicon wafers, or models. All of the 340 wafers in the SVT are double-sided, AC-coupled detectors, but their physical dimensions, pitch, and number of strips vary from model to model. The dimensions range from approximately 4.2 cm to 6.8 cm in length, and from 4.1 cm to 7.2 cm in width. All detector wafers are rectangular except for the model used in the arch portion of the outer layer modules, which is trapezoidal. The readout pitch is smallest in the inner layers, where resolution is most important. In layers $1-3$, the z-strip readout pitch is 100 μm; the physical pitch is 50 μm, where the intermediate "floating" strips are connected to the detector bias voltage (via a bias resistor) but are not directly connected to a channel of the readout chip. By using the capacitive charge division between the strips, we expect to obtain an instrinsic resolution on the z coordinate of about 12 μm. To minimize ambiguities in the pattern recognition, there is no z ganging in the inner layers. The ϕ-strip readout pitch is 50 μm in layer 1 and 55 μm in layers 2 and 3, with no floating strips. The wire bonds for these strips are the most demanding, and they are performed in two staggered rows of different heights.

In the outer layers the occupancy is lower and the hit resolution requirements are less demanding. The z pitch in layers 4 and 5 is 210 μm, and the ϕ pitch ranges from 82 μm to 100 μm, with one floating strip in both ϕ and z. We expect a ϕ resolution of about 10 μm and a z resolution of about 25 μm in the outer layers. We have reduced the large number of strips to be read out in the outer layers by ganging a fraction of readout channels ranging from 34% to 98%, depending on the sublayer.

The silicon wafers are glued and wire-bonded to intermediate flexible upilex fanout circuits, which are in turn glued and wire-bonded to the hybrid circuits. All together, there are about 150 K readout channels and 500 K wire bonds. The upilex fanouts allow us to mount the hybrids on the support cones at an angle to the silicon wafers. The hybrids and associated cooling are thereby kept out the tracking volume. The upilex is 50 μm thick, with a 150 nm Cr adhesion layer and 4.5 μm thick Cu traces, which have a resistance of 2 Ω/cm. The average radiation length is less than 0.05% at normal incidence. A useful feature of the fanouts is that they have an extension, which is cut off prior to wire-bonding to the hybrid, that is used for electrical testing. The traces on the upilex extension are large and relatively easy to probe. Before the detector-fanout assembly is glued and wire-bonded to the hybrid, we use this probing area to verify that the wire bonds between detectors and between the detectors and upilex are done properly.

The support structure consists of three main elements: an extremely rigid carbon-fiber space frame that connects the forward and backward cones; the cones themselves, which are kinematically mounted on the B1 magnets (to accomodate relative magnet motion during installation, or in an earthquake); and module support ribs and endpieces. (The space frame is not shown in Fig. 1.) The module support ribs are laser cut, with two thin carbon-fiber/epoxy outer pieces glued to a kevlar/epoxy piece sandwiched in between. Because the electrical conductivity of the carbon-fiber can affect the silicon, these outer parts are trimmed back so that only the kevlar is glued directly to the detector. Although kevlar by itself is quite strong, it can absorb moisture and deform. The carbon-fiber pieces prevent this potentially serious problem from occurring.

The silicon wafers are manufactured by Micron Semiconductor. The implants are biased through polysilicon bias resistors, with values ranging from 4 MΩ to 7 MΩ. The detectors deplete at voltages ranging from 15 V to 40 V, and their leakage currents are less than 100 nA/cm^2. The detectors are AC coupled; that is, there is an oxide layer between the each implant and its corresponding metal readout strip, with a capacitance of between 20 pF/cm and 40 pF/cm, depending on the detector model. The interstrip capacitance, which is important for determining the ENC of the amplifier noise level, is about 1 pF/cm (1 strip to single nearest neighbor). Other important parameters are the strip capacitance to the backplane, 0.2 pF/cm to 0.4 pF/cm; the implant resistance, 27 kΩ/cm to 55 kΩ/cm; and the metal trace resistance 6 Ω/cm to 13 Ω/cm. The capacitance of a single strip on the upilex to all others is 0.5 pF/cm.

To read out the detector, a new IC has been developed, which is discussed in a separate talk [4] at this conference. The analog front-end contains a preamplifier/shaper circuit that produces an output that is approximately logarithmic with pulse height, giving both good resolution at the low end and a large dynamic range. The peaking times are adjustable (100 ns, 200 ns, and 400 ns); lower values are used for the inner detector layers, where the occupancy will be the highest. A threshold is applied to the shaper output using a comparator; the comparator output (0 or 1) is then clocked at 15 MHz into a 12 μs trigger latency buffer. By clocking out the bits of this buffer and counting the number that are set, one obtains a time-over-threshold measurement. SPICE calculations indicate that, for $t_{\mathrm{p}} = 100$ ns, the ENC for a layer 1 ϕ (ohmic) side channel should be about 880 electons, while for the z (junction) side the ENC should be about 600 electrons. The largest noise is expected in layer 5, where SPICE simulations predicts an ENC of 910 electrons (z-side) and 1310 electrons (ϕ side) at a 400 ns shaping time.

We now have preliminary noise measurements based on laboratory tests of a a layer 2 half-module. (The modules are constructed in forward and backward sections, each of which has its own hybrid.) The hybrid in this test had a rad-soft prototype version of the readout IC, whose properties differ somewhat from those of the actual rad-hard IC to be used in production. The DAQ system was similar to the final BaBar SVT design, but a number of components were also in prototype versions. The shaping time was 100 ns. Figure 3 shows typical results of a threshold scan in which a fixed charge is injected at the front-end amplifier of each channel using the calibration circuitry of the readout chip. In these plots, the threshold decreases from left to right and is measured in ADC counts, where one count corresponds to a charge of about 410 electrons. For each data point shown, charge was injected 50 times, and the number of times in which the channel recorded a hit was counted. The sharpness of the turn-on provides a measure of the system noise; by fitting the results of the threshold scans to an error function, we have extracted rms noise values. Figure 4 shows the rms noise for all channels on the n and p sides of the layer 2 module. These measurements yield noise values that are ≈ 1070 electrons for the ohmic side and ≈ 860 electrons for the junction side at $t_{\mathrm{p}} = 100$ ns. These results, although about 30% higher than the predictions from a SPICE simulation, are quite encouraging and will be confirmed and possibly improved in an upcoming beam test in which the data acquisition components and power supplies will be closer to their final design.

At present, the detector design is complete and nearly all components are in production. Approximately one-half of the detector wafers have been delivered. Two prototype modules have been constructed, one for layer 2 and one for layer 5a. The BaBar detector will begin operation in early 1999.

References

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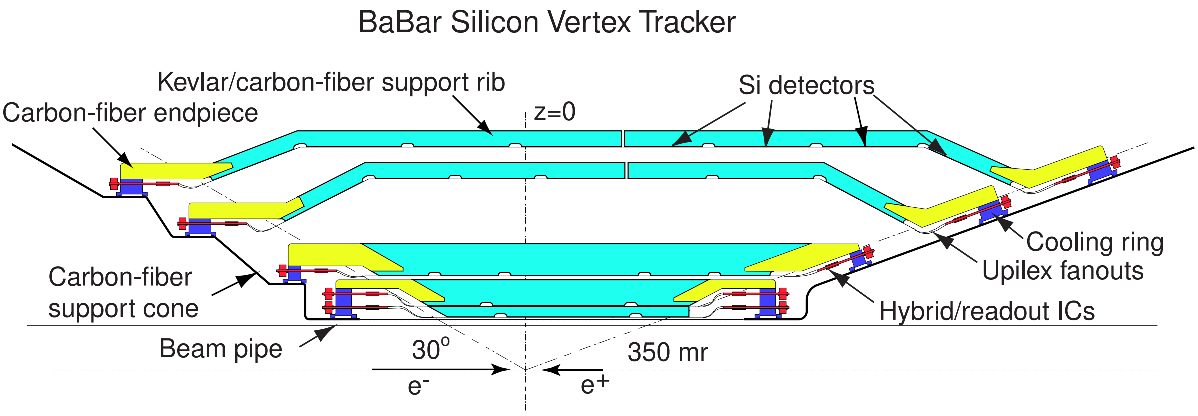

Fig. 1. BaBar Silicon Vertex Tracker, transverse view. Note the asymmetry of the detector with respect to the interaction point at $z = 0$. The modules are mounted to cooling rings on the carbon-fiber support cones; flexible upilex fanouts allow the hybrid circuits to be mounted at an angle with respect to the silicon detectors. Layer 1 and layer 2 detectors are rigidly joined together by the layer 1 support ribs.

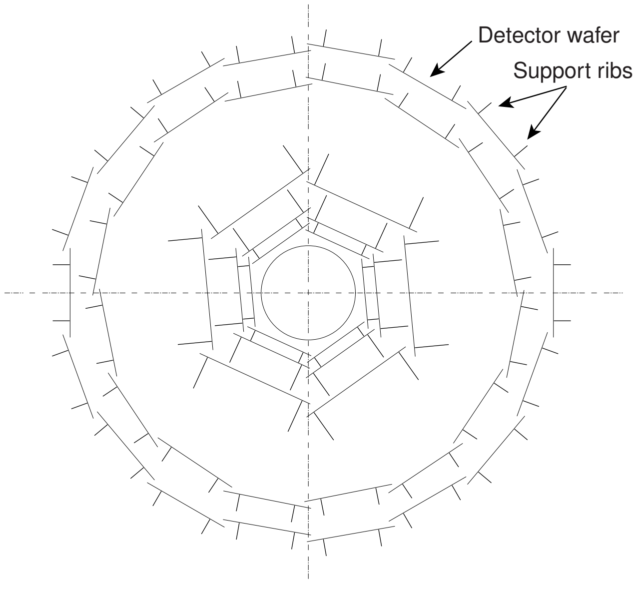

Fig. 2. BaBar Silicon Vertex Tracker: cross section view in the x-y plane.

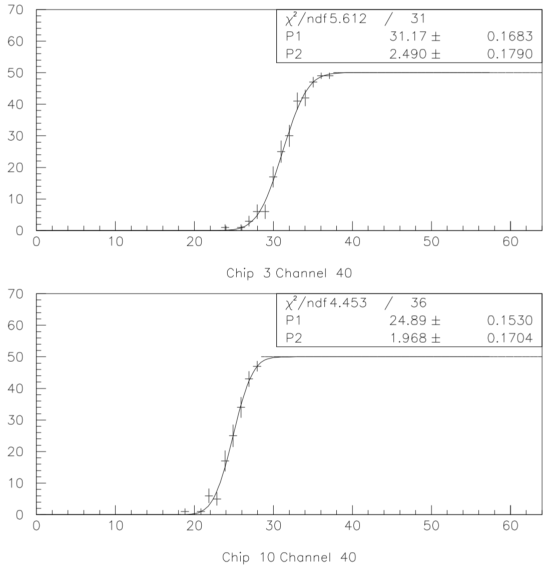

Fig. 3. Preliminary results from a threshold scan of a BaBar layer 2 module. As the threshold is decreased (left to right in the figure) the channel begins firing in response to a fixed input charge. The sharpness of the turn-on provides a measurement of the noise. The upper plot shows a channel on the n (ϕ) side, while the lower plot shows a channel on the p (z) side of the module, which has two wafers bonded to the hybrid.

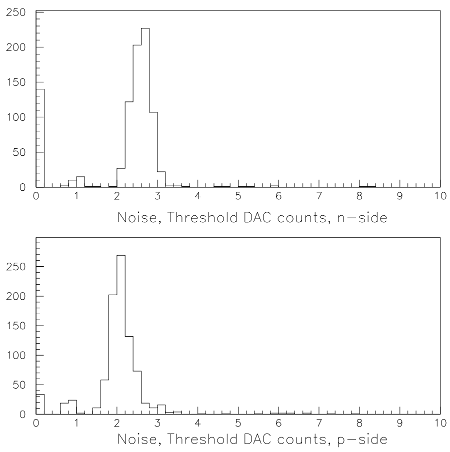

Fig. 4. Noise in units of the threshold DAC for all channels on the n-side (upper plot) and p-side (lower plot) of the detector. One threshold DAC count corresponds to about 410 electrons, giving a noise of 1070 electrons on the n-side and 860 electrons on the p-side at 100 ns shaping time. The peak at zero corresponds is due to a dead readout chip on the layer 2 hybrid.