Commissioning Module HDI Tests at UCSB

SVT Video Meeting
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- Testing Conditions
- Chip Power Consumption
- Digital Problems and Bad Channels
- Gain and Offsets
- Noise
- Current status

For gory details, see
`http://charm.physics.ucsb.edu/BaBar/HdiComm.html`

Testing Conditions

Test stand setup:

- Benchtop power supplies.
- UCSC MUX.
- LBL ROM.
- Clock frequency 40 Mhz.
- Duty cycle 50%.

HDI configuration:

- 1 forward and 1 backward Layer 2 h1 HDI.
- 7 rad hard V2 chips per side.

  Configuration A

  High gain selected

Chip Power Consumption

	Voltage	Current	Power
DVDD	5.0 V	450 mA	2.25 W
AVDD	5.0 V	330 mA	1.65 W
AVDD2	2.2 V	115 mA	0.25 W
Total per side (7 chips)			4.15 W

- 0.59 W per chip.
- 4.6 mW per channel.

Digital Problems

Forward HDI

- Rightmost chip on p-side is flaky.

  Corrupt trailer.

  p-side doesn't always read from right.

- Chip 10 (p-side)

  Data/status sometimes missing.

  Trigger tag is 0 (should be 1).

  Trigger time always 0.

- Chip 11 (p-side)

  Trigger time always 0.

- A few channels fire when masked off.

Digital Problems

Backward HDI

- Pad on chip 1 (n-side) visibly damaged by bonding accident at Aurel. Can't read chips 2-6 from left.
- 2 chips where many channels fire when masked off.

Bad Channels

Problem	Forward HDI		Backward HDI	
Dead	69	(7.7%)	0	(0%)
No response to Q inj.	141	(15.7%)	130	(14.5%)
Fires when masked off	10	(1.1%)	118	(13.2%)
Stuck on	2	(0.2%)	0	(0%)
Inefficient	1	(0.1%)	0	(0%)
Unknown	128	(14.3%)	1	(0.1%)
Total	351	(39.2%)	249	(27.8%)

Comments:

- Most of the problems with Forward HDI are due to 2 bad chips (254 out of 351).
- One chip on Backward HDI was good in testing before bonding to silicon. After bonding, all channels don't respond to Q injection.
- Above problem could be due to exceeding 5 V on AVDD or DVDD in power-up. Need CAEN supply for safety in production testing.

Gain and Offsets

Gain:

- Unbonded: 201 mV/fC.
- n-side bonded: 178 mV/fC.
- p-side bonded: 188 mV/fC.

Offset:

- Dispersion on a given chip: 13 mV.

Comments:

- The gain for chip 9 (p-side) on the forward HDI was anomalously low before bonding to the silicon (134 mV/fC). After bonding to the silicon, the gain went **up** 26% while the rest of the p-side chips went down about 6%.
- The numbers above are for 16 channels at a time. When done 1 chan at a time, the gain increases by 3.6% and the offset increases by 5 mV.

Noise

	t = 100 ns		t = 400 ns	
	counts	electrons	counts	electrons
Unbonded	1.2 to 1.5	390 to 490	1.0	330
n-side bonded	3.7 to 4.1	1370 to 1510	3.2	1180
p-side bonded	3.0 to 3.4	1050 to 1190	2.4	830

Comments:

- For a shaping time of 100 ns, the noise depends on the amount of charge injected. The range above is for CAL DAC values of 2 and 4 (n-side).
- For a shaping time of 400 ns, the noise is independent of the amount of charge injected.

Current Status

- The Forward HDI is fully bonded and tested.
- Bonding of the Backward HDI was completed yesterday. Will be tested by the end of the day.
- New CAEN power supply module arriving late today for testing.