# Electrical Testing of BaBar Silicon Vertex Detector Modules (Short Version)

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# 1 QC on modules during assembly

Testing will be a key part of module assembly. We are currently designing and constructing computer-automated test stands, and we have been evaluating our tests in detail using double-sided silicon wafers left over from construction of the silicon vertex detector for CLEO. All of our tests will be performed under computer control, using GPIB and VME instruments controlled with LabView and/or VxWorks software. The testing is described in detail in a separate document; here we outline the main elements.

Because the hybrids will not be available until over a year after module assembly has begun, much of the testing will be performed using a special, multipin probe. This probe, which will be lowered onto the extension portion of the upilex, enables us to access 256 channels on the upilex at one time. We have built a multiplexer circuit (the probe multiplexer) that is mounted directly on the probe; this system provides access to each readout strip independently under computer control. After gluing and wire-bonding the hybrids to the wafers, electrical testing will be performed by reading out the hybrid through VME.

The failure modes that we consider most likely are

- Excessive detector leakage current at the nominal bias voltage.
- Pinholes, or defects in the oxide layer between the readout and implant strips; these could be introduced by detector handling or by wire-bonding. Pinholes can also formed during the fabrication of the wafer, and we will have a map from earlier tests showing the strips that already have pinholes.
- Wire bonds that are shorted to a neighbor (leaning bonds).
- Interrupted signal traces on the detector (due, for example, to mechanical damage).
- Wire bonds that fail to connect (broken, misaligned, or nonsticking bonds).
- Interrupted traces on the upilex (mechanical damage).
- Failure of the detector to deplete properly.
- Failure of the hybrid.

Figure 1 shows the main components of the pre-hybrid test system, which we have prototyped and evaluated using CLEO silicon wafers. The system includes the probe; probe multiplexer, which consists of four 64-channel relay cards; an Instrument Switching and Relay Board Control card (this card is physically on top of the four relay cards); and a Relay Controller/Display, which allows for either manual or computer control of the relays. The power supplies for all of these components are run from high quality isolation transformers, and the Instrument Switching and Relay Board Control Card is opto-isolated from the Relay Controller/Display. The instrument switching portion of the Instrument Switching and Relay Board Control allows one to perform a wide variety of measurements without having to re-cable instruments. The outputs of the relay boards can be switched to a Keithley 487 picoammeter, to an HP4284A LCR meter, or to a LeCroy HQV820-M charge preamplifier. This board also allows one to access the bus line to which nonselected strips are connected.

from the shorting bars that can be placed over the upilex strips. The upilex shorting bar shown in the figure provides a simple mechanism to short together all AC strips on one side of the detector.

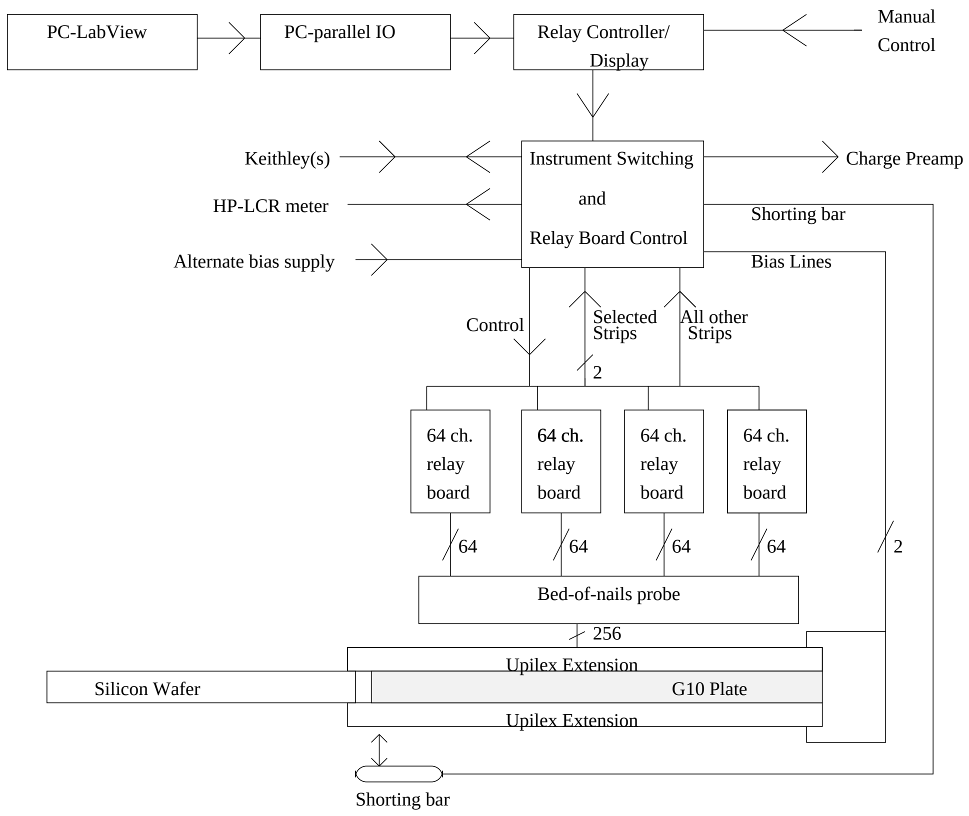


Figure 1: Schematic of test system showing the detector wafer with upilex, multipin probe, probe multiplexer, and computer control.

In many ways, the best test of the detector modules at any stage of assembly after the individual strips have been wire-bonded is to pulse the detector with an infrared LED. We have found that a Seimens SFH450 infrared LED is inexpensive, works extremely well, and can be purchased in a case that allows easy coupling to an optical fiber. The electrical signal to the LED has been controlled in two ways, first by simply driving it with an HP8116A pulser (with a current limiting resistor in series), and second, using an LED driver circuit that we built. This circuit can produce very fast high current pulses of variable width that may be useful when we want to investigate timing issues associated with the hybrid.

The assembly and testing sequence goes as follows.

- Immediately after receiving the Detector-Fanout-Assemblies (DFAs), and before beginning the wire-bonding process, we will check the integrity of the upilex fanout circuit. At this stage we are only able to check for shorts between upilex traces. This is accomplished by measuring the interstrip resistance. Note that a similar test will have already been performed as part of a more comprehensive upilex testing procedure. The goal of this test is to verify that no damage occurred to the upilex in transport from one laboratory to another.

- Wire-bond the bias and guard ring lines from the upilex to the wafer on both sides.
- Bias the detector and measure the total leakage current versus bias voltage. This measurement will be repeated before each of the testing steps described below.
- Wire-bond the inner row of bonds on the $\phi$ side to upilex. At this point the full length of the strip is not accessible, since the daisy-chain bonds haven't yet been done.
- Perform the overall test for shorts. This test is accomplished by measuring the resistance between each (bonded) channel and (i) all other channels or (ii) between each (bonded) channel and the $\phi$ side bias line. Shorts detected in test (i) can occur if two nearby wire-bonds touch. These can be fixed by combing the bonds. Shorts detected in test (ii) can be due to pinholes. Since the breakage of the AC capacitor which causes a pinhole is in general dependent on the applied voltage, we will likely perform the resistance measurement at a number of different voltages. The next test to be performed (see below) is a more comprehensive search for pinholes.
- $I$ vs. $V$ pinhole scan for bonded $\phi$ channels. In this test we measure the current flowing between each AC strip and the corresponding bias line as a function of applied voltage. Note that according to the detector specifications the AC capacitors are supposed to withstand a potential difference of 60 V.
- Interstrip resistance. Measure resistance between each bonded strip and its nearest and second nearest neighbor. The goal of this test is to find shorts between nearby channels. This measurement is redundant with the overall test for shorts described above, however it will be useful in pinpointing the location of any such short.
- Interstrip capacitance measurement for bonded $\phi$ strips. Measure capacitance between each bonded strip and its nearest or second nearest neighbor. Disconnected bonds will result in abnormally low values of interstrip capacitance.
- Wire-bond outer row of bonds (over the top) on the $\phi$ side to upilex.
- Repeat battery of tests on $\phi$ side : (i) overall test for shorts, (ii) IV pinhole scan, (iii) interstrip resistance, (iv) interstrip capacitance.
- Wire-bond daisy chain bonds between different silicon wafers in the same DFA, $\phi$ side.
- Repeat battery of tests on $\phi$ side : (i) overall test for shorts, (ii) IV pinholew scan, (iii) interstrip resistance, (iv) interstrip capacitance.
- LED scan, $\phi$ side. Using a precision $xy$ stage and the IR LED, we will scan the LED light over the whole detector. The channel corresponding to the position of the LED light will be connected to the charge amplifier through the scanner. The output of the charge amplifier will be read-out through an analog-to-digital-converter. This test will be useful in verifying the integrity of the silicon wafers and will also detect disconnected wire-bonds.

- Wire-bond all channels on $z$ side.
- Perform battery of tests on $z$-side : (i) overall test for shorts, (ii) IV pinhole scan, (iii) interstrip resistance, (iv) interstrip capacitance.
- Repeat battery of tests on $\phi$ side to insure that handling of detector did not introduce additional damages on the $\phi$ side.
- Measure bulk capacitance as a function of bias voltage. This is accomplished by shorting all AC strips on each side together using shorting bars placed on the upilex extensions and measuring the capacitance between the two sides. This measurements verifies the value of the depletion voltage.
- Measure capacitance between each strip (on both sides) and all other strips, shorted together, on the opposite side. This measurement is sensitive to broken wire bonds.
- LED scan on $z$ side.

We now describe the series of tests to be performed with the detectors bonded to the hybrids. Before committing to bonding a given hybrid to a DFA, we will repeat the set of tests on the hybrid performed in Milan, to make sure that the hybrid was not damaged in shipping. We will first verify the integrity of the communication between the DAQ board and the hybrid, and we will then perform threshold and charge injection scans.

Once the hybrids are bonded to the DFAs, we will repeat the measurement of leakage current as a function of bias voltage to verify that the detectors were not damaged in the wire bonding process and that the bias bonds are in place. We will then again perform the same hybrid tests (communication, theshold and charge injection scans) that were performed on the bare hybrids prior to wire bonding. We will then perform an LED scan of the DFAs, reading out the detectors through the standard BaBar readout chain. We envision that in this testing phase we will make use of a prototype BaBar-SVT power supply system.

In conclusion, we have designed and evaluated a set of tests that will allow us to maintain good quality control during the SVT module assembly process. All of our tests were studied with a CLEO silicon wafer and are effective in finding the types of problems that are likely to occur. The tests are sufficiently broad that unforseen problems that can significantly affect the detector operation should be evident. The overlap among the tests should help us to diagnose the nature of any new problems.