Electrical Testing of BaBar Silicon Vertex Detector Modules

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1 Introduction

This document describes the electrical tests that we plan to perform during assembly of BaBar silicon vertex detector (SVT) modules at UCSB. Module assembly will require approximately two years. We will begin work on the barrel modules, which will be used in the three inner layers of the SVT, starting in August 1996 and ending in July 1998. Arch modules, which will be used in the two outer layers of the SVT, will be assembled in Pisa starting in September 1996 with completion scheduled for August 1998. Testing will be a key part of module assembly. Since the SVT is crucial to the measurement of CP violating asymmetries in the BaBar experiment, and because the SVT will be essentially inaccessible once installed, we need to have very high confidence in our assembly procedures.

At UCSB, we are designing and constructing two computer-automated test stands, and we have been evaluating our tests in detail using double-sided silicon wafers left over from construction of the silicon vertex detector for CLEO. All of our tests will be performed under computer control, using GPIB and VME instruments controlled with LabView and/or VxWorks software. We regard automation of the testing as essential, since our goal is to keep the testing time as short as possible, to make the tests easy to perform, and to have all results automatically logged on the computer.

From the perspective of testing, module assembly can be divided into two phases. The first consists of the steps prior to gluing and wire-bonding the hybrid circuits to detector wafers. At UCSB, we will receive from Pisa detector wafers that have already been glued to each other and to the flexible upilex readout circuits. These objects are called detector-fanout assemblies, or DFAs. Our most time consuming activity during phase 1 will be wire-bonding the detector wafers to the upilex readout circuits. The detector cannot be read out conventionally at this stage, and electrical testing must therefore rely on special probes. In section 3.1 we describe a UCSB-built multipin probe that will enable us to access 256 channels on the upilex at one time. The second phase of module assembly begins with gluing and wire-bonding the hybrids to the wafers; electrical testing from this point on will be performed by reading out the hybrid through VME in a manner similar to what will be done in the actual experiment.

The schedule for delivery of the hybrid has major implications for our approach to testing. Because a major component of the hybrid is a newly designed, radiation-hard readout chip, the hybrids will not be available until well after module assembly has started. The hybrids for layers 1–3 are scheduled for delivery to UCSB around the end of 1997, more than a year after module assembly has begun. However, it is essential that we verify as early as possible that our assembly steps during phase 1 have been carried out successfully. In particular, we need to determine whether the wire bonds are good and whether the wire-bonding process or other detector handling procedures cause damage to the detector in any way, for example, by introducing pinholes in the thin, insulating layer between each detector AC readout strip and its corresponding implant.

Recognition that we need to perform extensive electrical testing before we can read out the detector through the hybrid resulted in a modification to the design of the upilex circuits. These circuits, made of a thin, flexible kapton-like material on which the traces are printed, are extended beyond what is required to connect the detector wafers to the hybrids. In addition, in the extension portion of the upilex, the traces fan out into a region called the "parking lot", where they become broader and have larger separation. The traces are organized into Christmas-tree-like patterns where probes can be brought down to make electrical connections. Just before gluing the upilex to the hybrid circuit, this extension will be cut off to the appropriate length.

In the following sections, we describe the equipment and procedures that we have developed for electrical testing. In section 2, we discuss the detector model and expected failure modes that we used to design our tests. In section 3, we describe how the phase 1 (pre-hybrid) tests are implemented in detail. We discuss the probe for making the electrical connections to the upilex, the equipment and circuits used in each test, and some of the results from evaluations of the tests that we have performed using CLEO silicon wafers. In section 4, we give the detailed sequence of the phase 1 tests. We separate discussion of the sequence of the tests from their description because some of the tests are performed multiple times during module assembly. Section 5 describes the tests to be performed once the hybrid is attached to the detectors.

2 Concepts for electrical tests

During module assembly, we plan to verify the full functionality of each detector strip and its associated readout path. In this section, we describe the electrical characteristics of the detector and the failure modes that we consider to be most likely. Using this basic information, we then list a set of tests that should reveal any of the expected problems. The tests overlap to some extent and are therefore partly redundant. However, if failure modes occur other than those we anticipate, having the ability to perform these tests could help us to pinpoint the problem more quickly.

Figure 1 shows schematically the main features of a detector wafer, as well as the signal readout path. The substrate detector material is high-resistivity n-type silicon. Both electrons and holes produced by an ionizing particle are collected, the electrons on the n^+ implant strips and the holes on the p^+ implant strips, which run in the orthogonal direction. The detector is depleted by applying a reverse bias voltage between the n-side and p-side bias lines. These lines are connected to the implant strips via polysilicon bias resistors (one per strip), whose resistance is about 8 $M\Omega$. The implants are not directly coupled to the readout electronics, but are instead AC coupled through an intrinsic capacitor that is part of the detector. An oxide layer overlaid on top of the implants and substrate provides the dielectric; aluminum readout strips, sometimes called AC strips, are laid on top of this oxide directly over their corresponding implant strips. In the absence of pinholes, the capacitors prevent DC leakage current from the detector from affecting the readout electronics.

On the side of the detector that reads out the ϕ coordinate, the strips run in the z direction, and there are daisy-chain wire bonds from wafer to wafer. In layers 1 and 2, the two forward detectors in each sextant are wire-bonded and the two backward detectors are wire-bonded in this manner. In layer 3, there are three forward and three backward detectors; each of these groups is daisy-chained together with wire-bonds on the ϕ side. Thus, on the ϕ side, the wafer's signal strips themselves carry the signals to bond pads at the end of the wafer, where another set of wire-bonds connects the strips to bond pads on the upilex readout circuits. On the side of the detector that reads out the z coordinate, the

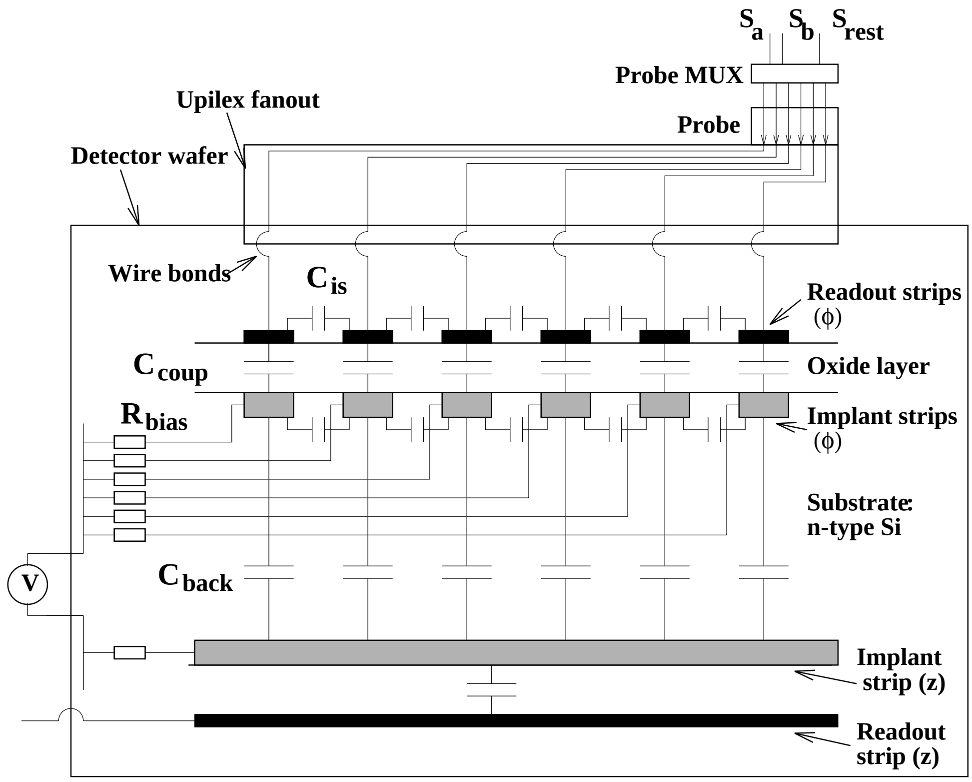


Figure 1: Schematic of detector wafer, upilex, and probe.

arrangement is different, because the strips run across the wafers (perpendicular to the z direction). The bond pads are located along the two long sides of the wafers. Wire-bonds connect these pads to pads on a piece of upilex that is glued down directly to the surface of the wafer; the strips on the upilex carry the signals in the z direction along the wafers and to the hybrids.

With this picture in mind, we can make a list of failure modes or conditions for the pre-hybrid phase of the assembly:

- Excessive detector leakage current at the nominal bias voltage.
- Pinholes, or defects in the oxide layer between the readout and implant strips; these could be introduced by detector handling or by wire-bonding. Pinholes can also formed during the fabrication of the wafer, and we will have a map from Pisa showing the strips that already have pinholes.
- Wire bonds that are shorted to a neighbor (leaning bonds).
- Interrupted signal traces on the detector (due, for example, to mechanical damage).
- Wire bonds that fail to connect (broken, misaligned, or nonsticking bonds).
- Interrupted traces on the upilex (mechanical damage).

- Failure of the detector to deplete properly.

Once the hybrid is attached and wire-bonded, a whole separate set of tests is required to exercise the full functionality of the hybrid. These tests will be discussed in Section 5.

We now briefly consider how one can find the problems in this list. Leakage current at the nominal bias voltage is easily measured, since it only requires that we bond the detector bias lines and apply the bias voltage. In fact, the bias and guard ring lines will be the first that we wire-bond to the upilex, so we will be able to perform this test very early in module assembly.

We will test for pinholes in the oxide layer of each strip by applying a voltage between the readout strip and the bias line on the same side of the detector and measuring the current. We have built a multiplexer circuit (the Probe Multiplexer) that is mounted directly on our probe; this system provides access to each readout strip independently under computer control.

Accidental contact between nearby wire bonds is a serious concern. In layer 1, the ϕ-side wire bonds have a pitch of 50 μm, in layers 2 and 3 the ϕ-side wire bond pitch is 55 μm, and in layers 1–3 the z-side wire bond pitch is 100 μm. The ϕ-side bond pads are staggered, so that alternate bonds will have a length of about 2.2 mm for the "inner bonds" and about 2.6 mm for the "outer bonds." The longer, outer wire-bonds will also be higher, and they have a tendency to lean and potentially come into contact with their nearest-neighbor outer bonds. We will need to identify when this occurs and correct the shorts by "combing" the bonds. To find touching bonds, one can simply measure the resistance between nearby pairs of signal strips. The Probe Multiplexer has the ability to select two strips S_a and S_b (see Fig. 1), where strip S_b is the first, second, or third nearest neighbor to strip S_a.

We can combine the pinhole test and the search for shorts in the following way. We use the fact that the Probe Multiplexer brings out not just two strips S_a and S_b, but all the remaining strips that the probe touches onto a bus line called S_{rest}. Figure 2 shows the configuration for this inclusive search to determine whether a given strip has a pinhole or is shorted to any other strips. The idea is simply to see if there is low resistance between a given signal strip and any other strip or implant on the same side of the detector. If a low resistance is found, the tests described in the previous two paragraphs can be performed to determine where the problem is.

DC measurements will not tell us whether the signal path from the readout strip to the upilex is interrupted, because the readout strip is AC-coupled to the implant. However, there are two measurements that will demonstrate continuity. The first is to measure the capacitance of the strip to its implant. If the continuity is broken at any point along the detector, the capacitance will be correspondingly reduced. (An interstrip capacitance measurement will also work.) For example, if the interruption is at a daisy-chain wire-bond on the ϕ side, the reduction in capacitance will be very distinctive. To perform this measurement, we short all of the readout strips together on the opposite side of the detector (by placing a shorting bar on the upilex traces in the extension region), and measure the capacitance between the given signal strip and the shorted strips on the other side. With the detector unbiased, the capacitance associated with the depletion layer is absent, so the capacitance will be dominated by that between the signal strip and its implant. This measurement configuration is shown in Fig. 3. As discussed in Section 3.4, we have shown that this technique

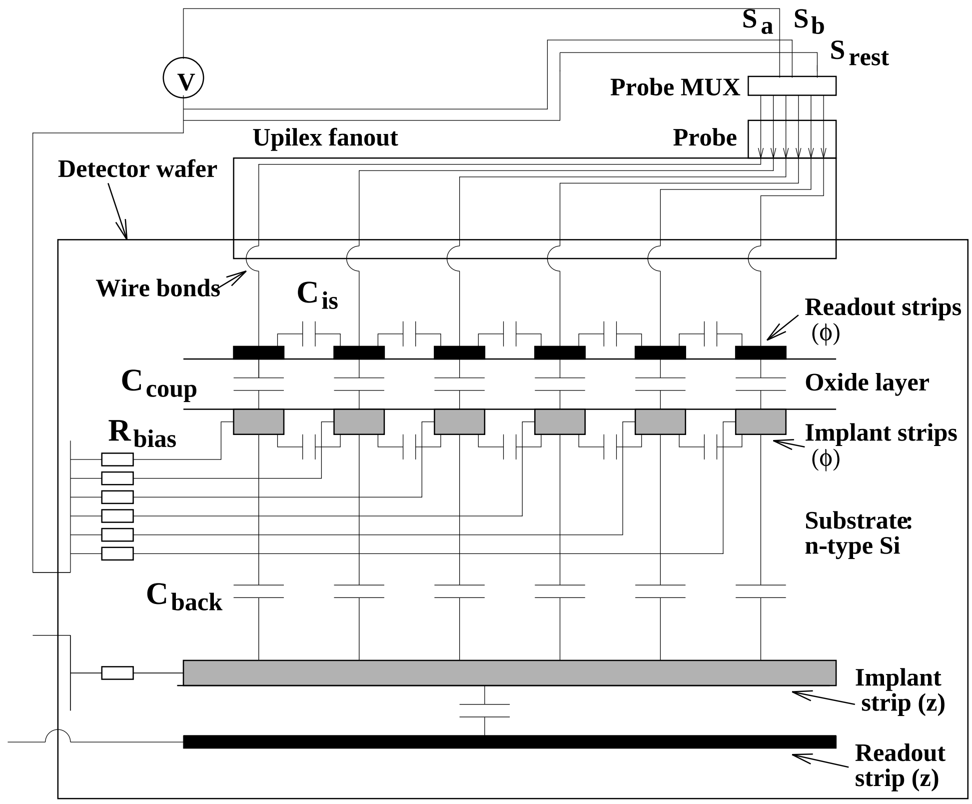


Figure 2: Configuration to search for pinholes and shorts simultaneously.

works quite well. In fact, this measurement also reveals pinholes and shorts to neighboring channels—almost any problem affects the capacitance in some way—so one can correlate the results of this measurement with those of the DC measurements discussed above.

The second method for determining whether the signal path is continuous is to pulse the detector with light from an infrared LED and to verify that there a signal. We have found that this approach also works well, and we can produce and observe analog signals ranging from that of a minimum ionizing particle (min-I) to over 25 times min-I. The equipment for this test consists of an LED pulser, a simple optical system, a computer-controlled xy stage to scan the optics over the detector, and a LeCroy charge-sensitive preamplifier. The illuminated spot from the LED covers two strips and can be made smaller if necessary. As with all of the measurements, we use computer control and the Probe Multiplexer to select the detector strip that is connected to the preamplifier.

The infrared pulser system verifies the full functionality of the detector, including depletion. We can make plots of the pulse height vs. bias voltage to show that we are obtaining a saturated pulse height, thereby showing that the detector is fully depleted.

As discussed in the following sections, the switching from one measurement configuration to another is performed under computer control using high-quality relays. No moving of cables is required once the detector is placed in the test fixture and the basic connections are made.

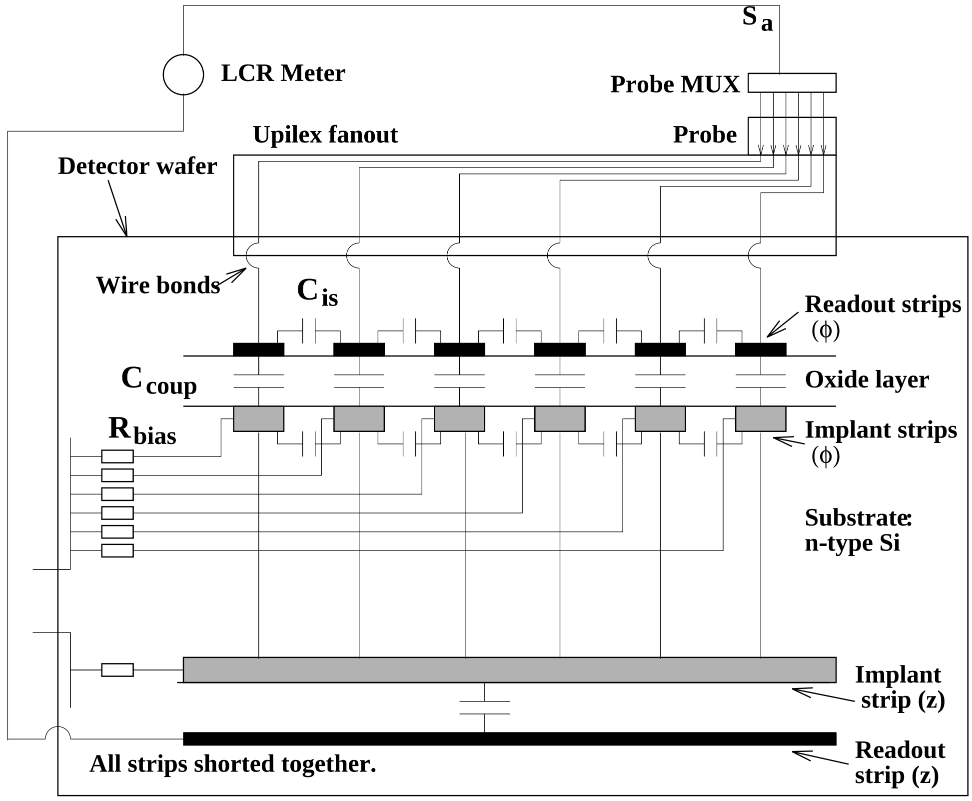


Figure 3: Configuration to search for interrupted strips using capacitance measurements.

3 Description of tests prior to hybrid bonding

In the following sections, we describe in detail the setup for tests prior to attaching the hybrids to the detectors. While these tests are being performed, the detector wafers will be held in a fixture called the ring frame, which is the same protective fixture used for all operations during module assembly, including wire-bonding. The electrical tests will be performed in a large metal box to keep out light. There will actually be two such boxes, each equipped with an xy stage for scanning a small optical system (coupled to an LED with a fiber) across the detector wafers. One of the boxes will be used for testing prior to attaching the hybrid; the other will be used for testing after the hybrid is attached. Our goal in having two setups is to enable parallel testing of modules at different stages of assembly, since there will very likely be a great deal of time pressure to complete the construction.

The pre-hybrid tests are controlled by a PC with LabView, which is interfaced through National Instruments data acquisition cards to the Probe Multiplexer, xy stage, charge-sensitive preamplifier, and GPIB instrumentation (picoammeter, LCR meter, and digital oscilloscope). The after-hybrid tests will be controlled by a computer running VxWorks in a VME crate. We will flow dry air into the boxes to keep the humidity low, and we will automatically record both temperature and humidity during the measurements.

The following sections describe the Multipin Probe, the Probe Multiplexer, DC measurements, AC measurements, and infrared LED measurements.

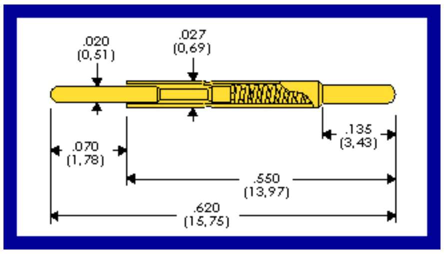
3.1 Multipin ("Bed-of-Nails") Probe

To perform the electrical tests described in Section 2, we need to make reliable electrical connections to the individual AC strips, as well as to the bias lines. As we discussed in Section 1, the upilex circuit glued to the detector wafer has a temporary extension which can be used for testing, and which will be removed (cut) just before the hybrid is attached. On this extension the traces, which normally have a pitch of $\approx 50\ \mu$m, are fanned out in Christmas-tree-like patterns to a pitch of $500\ \mu$m, and a width of $300\ \mu$m. The minimum length of a branch of the Christmas tree is 3 mm. For mechanical stability, this extension will be glued to a G10 plate that is part of the ring-frame structure that holds the detector. Connections to the AC strips can then be made through a probe that comes into contact with the fanned-out traces. In this section we describe a probe that we have designed and prototyped at UCSB, the "bed-of-nails" probe.

Size SS40 Probe

.039" (0.99) Centers
.050" (1.27) Maximum Travel

Size SS40 Spring Contact Probe



Spring Force Options

	1.8 oz. Spring	2.4 oz Spring
Preload Spring Force	1.2 oz. (34g)	1.4 oz. (40g)
Rated Spring Force*	1.8 oz. (51g)	2.4 oz. (68g)
Material	BeCu, Gold Plated	Stainless Steel, Gold Plated

* at .050 (1.27) travel

Figure 4: The spring-loaded pins used in the UCSB bed-of-nails probe. We have selected the 1.8 oz spring force option. From http://www.idinet.com/ss40.html.

The bed-of-nails probe uses spring-loaded gold plated pins from Interconnect Devices (Figure 4). These pins are positioned in a fixture to an accuracy of about $25\ \mu$m. The upper plate of the fixture, which holds the pins, can then be lowered onto the lower plate, so that the pins press onto the upilex Christmas-tree structure and make electrical contact. The upper plate is guided by four ball bearings mounted on vertical posts. Each pin of the probe is connected through a wire to a standard 64-pin connector; this connector accepts one of a set of relay boards that are discussed in the next section, where we describe the Probe Multiplexer. The required compression force is ≈ 50 g per pin (see Figure 4). The probe and the upilex are aligned using a set of reference holes that are built into the design of the upilex extension for this purpose. In Figure 5 we show a drawing of one upilex Christmas-tree, and the positioning of the pins of the "bed-of-nails" probe.

A prototype probe, with 128 pins, has been built and tested at UCSB. Most of the measurements performed on CLEO silicon wafers discussed in sections 3.3, 3.4, and 3.5

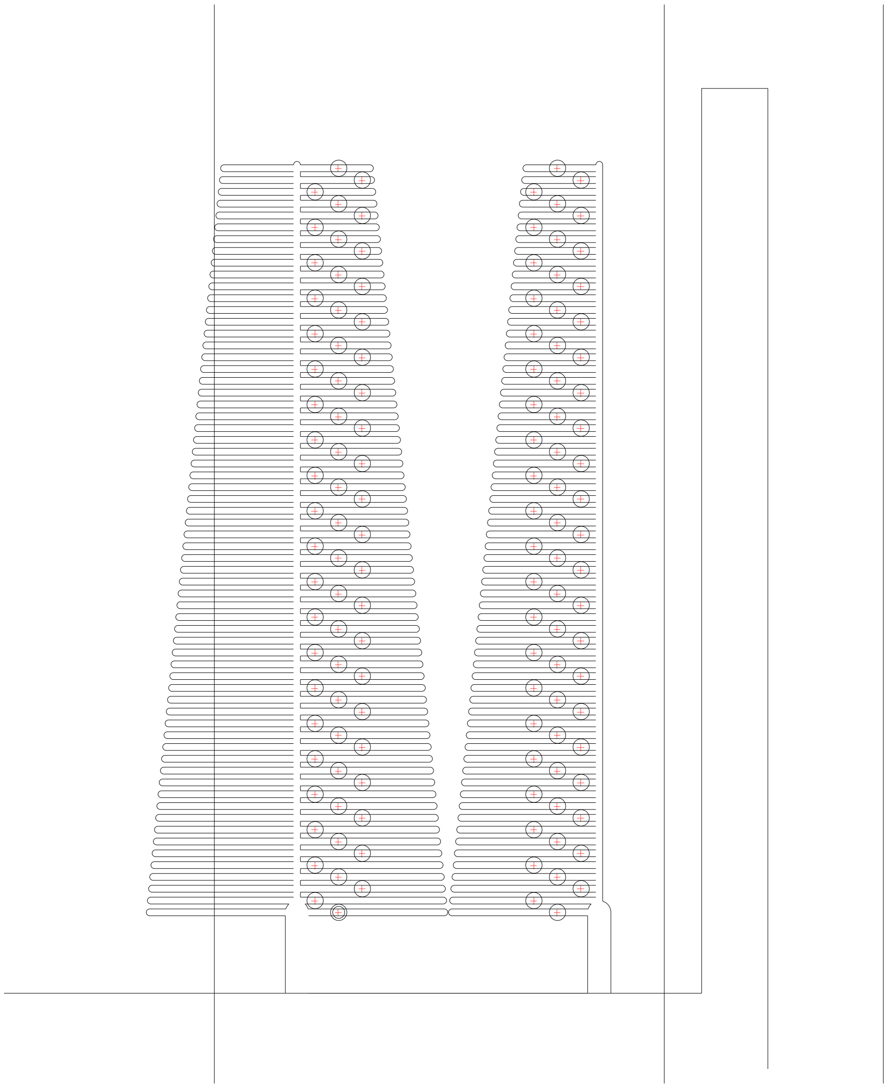


Figure 5: Footprint of the upilex Christmas-tree (horizontal lines) and the pins of the "bed-of-nails" probe.

were performed using this probe and the probe multiplexer circuit described in section 3.2. The World Wide Web site http://charm.physics.ucsb.edu/BaBar/probe.html. has several photographs of the prototype probe.

The reliability of the connections between the pins and the upilex traces has been tested and found to be very good. The test is carried out by repeatedly raising and lowering the probe from the upilex and measuring the resistance between each pin and its nearest neighbor when all traces on the upilex are shorted together. (This test is performed very quickly using the LabView-controlled probe multiplexer circuit.) The resistance between a pin and a trace is measured to be $\approx 3.5\ \Omega$, which is small compared to the resistance of the trace itself. The capacitance between adjacent channels is ≈ 2.6 pF. If required, offsets like this can be measured and subtracted out of the affected measurements, but this small capacitance is irrelevant for our tests.

If tests using the probe indicate missing or interrupted continuity on a particular channel, one might suspect that the probe pin for that channel is not making a good connection to the upilex trace. It will be possible to verify this connection by placing the shorting bar across the upilex traces, as discussed above. In fact, we may perform a test with the shorting bar as part of the standard procedure for lowering the probe to the upilex.

Contacts between the spherical tips of the probe and the traces on the upilex cause shallow indentations in the traces. These indents do not impair the ability of the trace to make electrical contact in subsequent probe tests. The indents cannot affect the detector operation in the experiment, because this extention part of the upilex is removed prior to attaching the hybrid.

There are seven readout chips on each side of a hybrid in layer 1 or 2, and ten on each side of a layer 3 hybrid. Each readout chip has 128 channels, and each chip is mapped onto one Christmas-tree on the upilex extension (Figure 5). We believe that we do not need access to all thousand or so channels on each side of the detector simultaneously. We have therefore decided that the probe to be used in production testing will have 256 pins and will cover two Christmas-trees. We are investigating a stepping motor system to translate the probe pins from one region to the next on the upilex extension. Should this prove to be too cumbersome, we will just move the probe by hand.

3.2 Probe multiplexer circuit

The Probe Multiplexer is the device that allows one to select the strips to be tested and to connect them to the testing equipment. Figure 6 shows the Probe Multiplexer, which consists of four 64-channel relay cards; an Instrument Switching and Relay Board Control card (this card is physically on top of the four relay cards); and a Relay Controller/Display, which allows for either manual or computer control of the relays. The power supplies for all of these components are run from high quality isolation transformers, and the Instrument Switching and Relay Board Control Card is opto-isolated from the Relay Controller/Display.

Channel switching on the relay boards is implemented using Aromat TK relays, which are compact and reliable. The 256 channels of the bed-of-nails probe are connected to four 64-channel relay boards, shown in Figure 7. Through these cards one can make simultaneous connections to (i) a selected primary strip; (ii) a secondary strip, which is the first, second, or third nearest neighbor of the selected strip; and (iii) all remaining strips shorted together. Figure 7 shows that when a strip is not selected, it is switched to a bus line. The relays are activated by a bit pattern that is loaded into the series of shift registers.

The instrument switching portion of the Instrument Switching and Relay Board Control, shown in Fig. 6, allows one to perform a wide variety of measurements without having to re-cable instruments. The outputs of the relay boards can be switched to the Keithley 487 picoammeter, to the HP4284A LCR meter, or to a LeCroy HQV820-M charge preamplifier. This board also allows one to access the bus line to which nonselected strips are connected (UNUSED STRIPS). The lines labelled “Z Side Strips” and “Phi Side Strips” come from the shorting bars that can be placed over the upilex strips. When placed across the strips on the upilex extension, they provide a simple mechanism to short together all AC strips on one side of the detector.

The schematic of the instrument switching portion of the Instrument Switching and Relay Board Control card is shown in Figure 8. Aromat relays are also used here to switch between

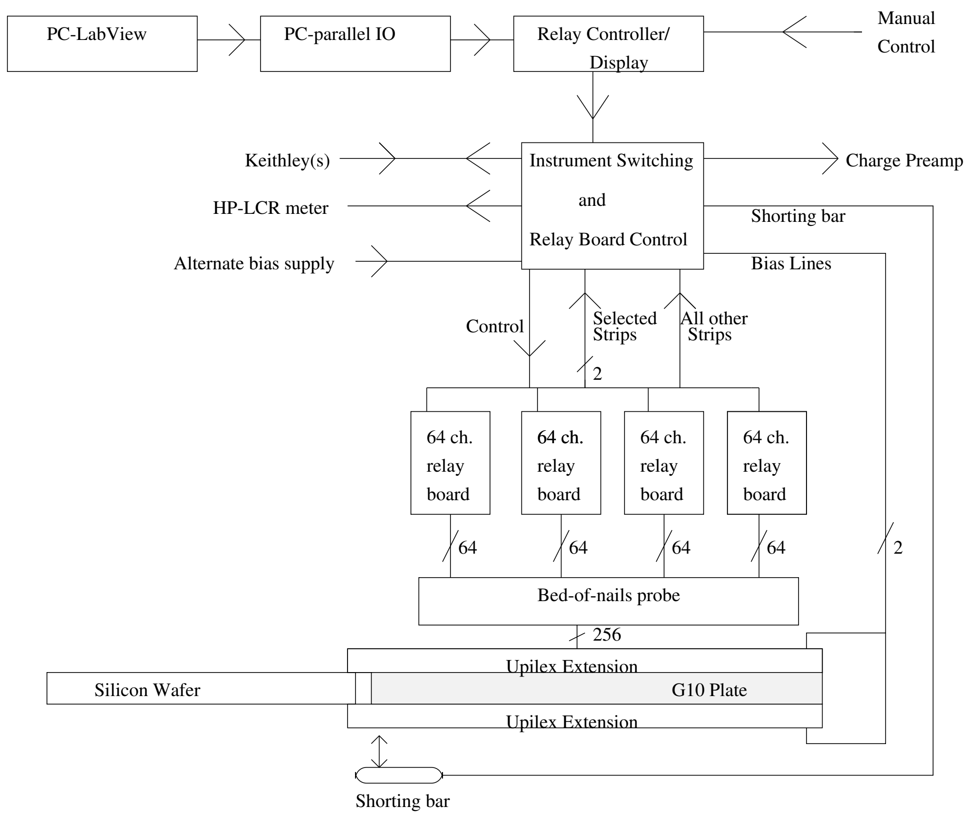


Figure 6: Block diagram of the Probe Multiplexer system. The HP4284A LCR meter and the Keithley 487 Picoammeter/Voltage Sources are also controlled by Labview through a GPIB interface. The output of the charge pre-amplifier (LeCroy HQV820-M) is fed to an ADC in a National Instruments PC+ data acquisition card.

different channels. This card will allow for automatic setup, with no need for re-cabling, for all the tests that are presently envisioned. For example, a measurement of leakage current as a function of bias voltage can be made using the Keithley ammeter/voltage source through relays K16 and K18 (Figure 8). An I vs. V scan of a coupling capacitor on the ϕ side can be performed by closing relays K16 and K25, and then ramping Keithley No. 1. The same tests can be also performed with the detector biased, where the bias voltage is provided by the Alternate Bias Supply J18 through relays K21 and K22.

A prototype Probe Multiplexer has been built at UCSB. Most of the measurements on CLEO wafers discussed in sections 3.3, 3.4, and 3.5 were performed using the prototype system.

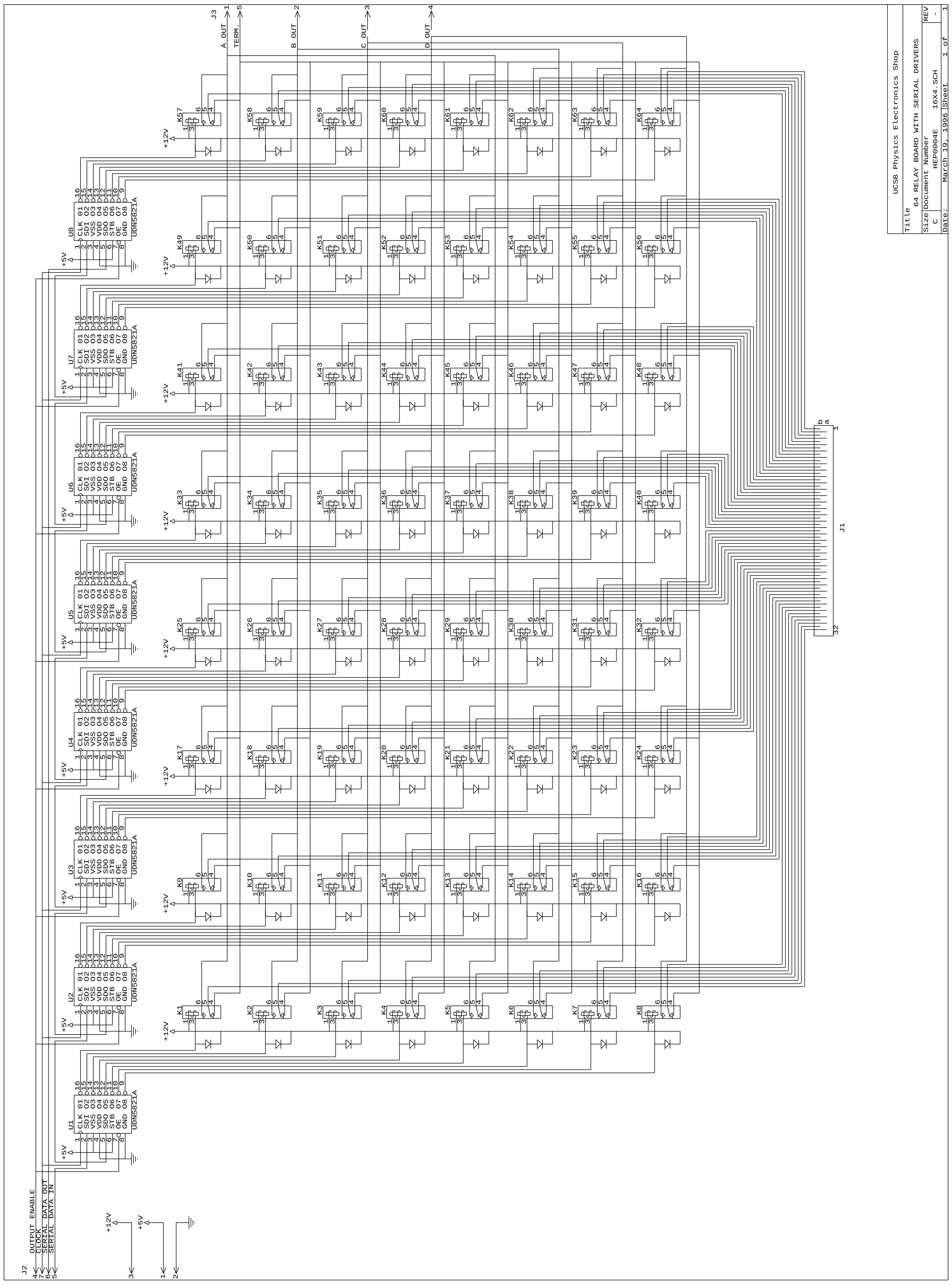


Figure 7: Schematic of a 64-Channel Relay Board. The Aromat relays are controlled by a bit pattern that is clocked through a set of shift registers. The strips that are not selected are connected to a bus line that is also accessable.

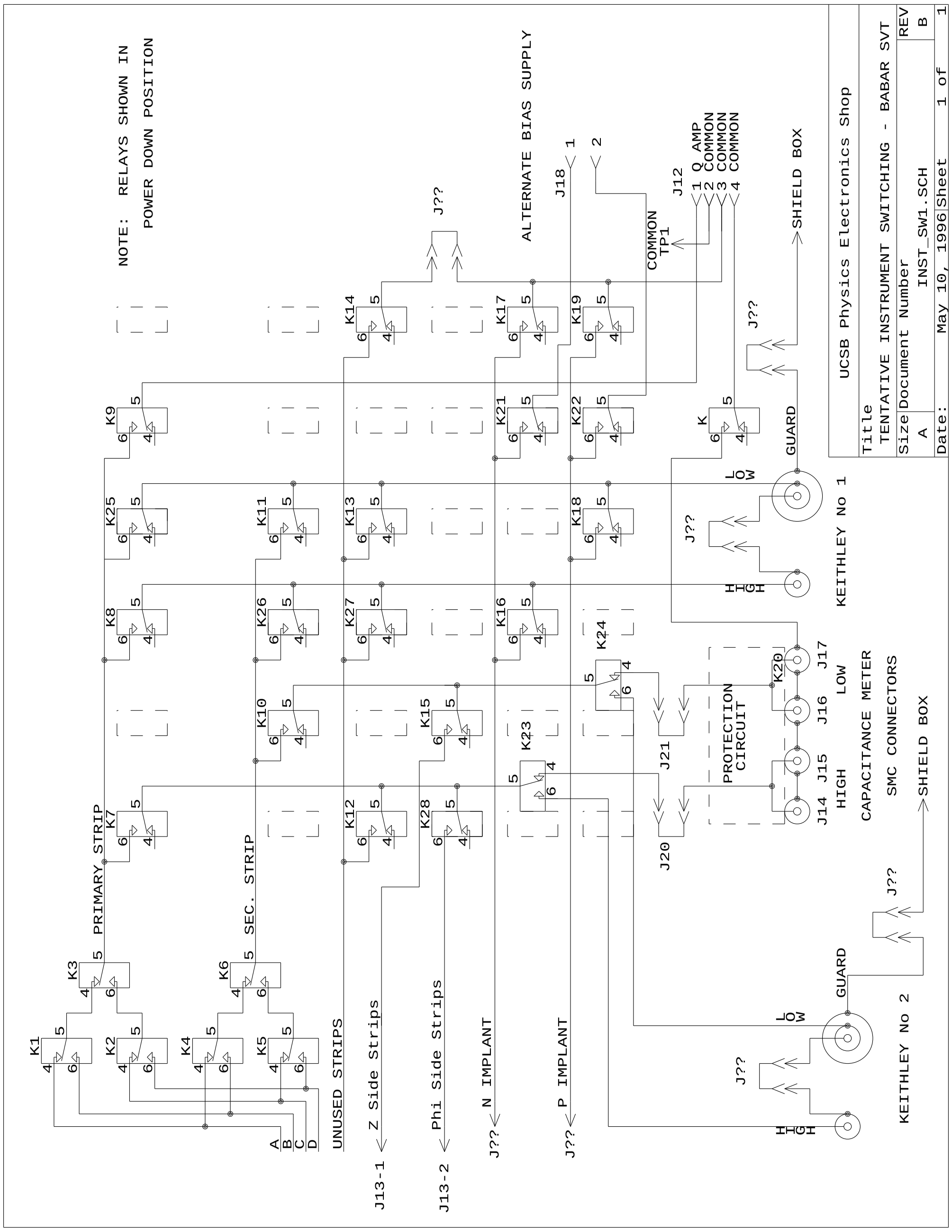


Figure 8: Schematic of the instrument switching portion of the Instrument Switching and Relay Control card. The protection circuit for the capacitance meter is necessary because the HP4284A can be damaged if the potential difference between its inputs exceeds 42 V. The protection circuit that will be used is from HP-Technical Note 346.

3.3 DC measurements and evaluation with CLEO silicon wafer

The DC measurements will be performed with a Keithley 487 Picoammeter/Voltage source. The 487 is GPIB-controlled, and the voltage source has a range of 500 V and a current limit that can be set to either 25 μA or 2.5 mA. For our purposes the lower range is appropriate.

As discussed in Section 2, there are several key tests that we will perform with very simple DC measurements. To prepare our setup and to verify that we can perform these measurements with our probe and probe multiplexer, we have studied a silicon wafer left over from the CLEO silicon vertex detector project. The CLEO wafer is mounted in a G10 frame, which also holds the upilex readout circuits onto which the probe pins are lowered. Both the ϕ and z sides of the detector are read out with upilex. The CLEO wafer is double metal on the z side, so the same type of upilex that is used on the ϕ side works for the z side. The bond pads on each side of the wafer have about a 100 μm pitch, whereas those on the upilex have 50 μm pitch. The bonds were made so that there are groups of adjacent strips on the wafer that also immediately adjacent on the upilex; there is then a gap of unbonded upilex strips followed by another series of bonded strips. The bias lines on the upilex do not go through the probe, but instead come out on separate wires to a Molex connector, into which we plug a connector from the Keithley supply.

3.3.1 Leakage Current vs. Bias Voltage

The most basic measurement, and the one we will perform as soon as we bond the bias and guard rings to the upilex, is that of leakage current (I_{leak}) vs. bias voltage (V_{bias}). The sequence of measurements is performed automatically under LabView control and is programmed in 10 V steps. The data are obtained from the Keithley 487 via the National Instruments GPIB interface in the PC. We plan to opto-isolate this interface in the near future using a commercial GPIB opto-isolator. The Keithley is powered from a high-quality isolation transformer.

3.3.2 Pinholes

As noted in Section 2, we will search for pinholes by applying a voltage between the signal strip and the bias line on the same side of the detector. Pinholes in the CLEO detector wafers are not always evident when a small voltage is applied; that is, the pinholes do not behave just like a dead shorts through the insulating layer. Typically, there is a threshold voltage below which there is no breakdown; even above this threshold, the pinhole does not necessarily behave as a dead short. We have not yet decided on the voltage at which we will perform this test. Figure 9 shows the current vs. strip number measured at 10 V on a CLEO wafer using our probe and probe multiplexer. Several peaks corresponding to pinholes are evident. This measurement was performed with an unbiased detector. We have the ability to bias the detector at the same time, but we have not decided on whether to do this during the testing.

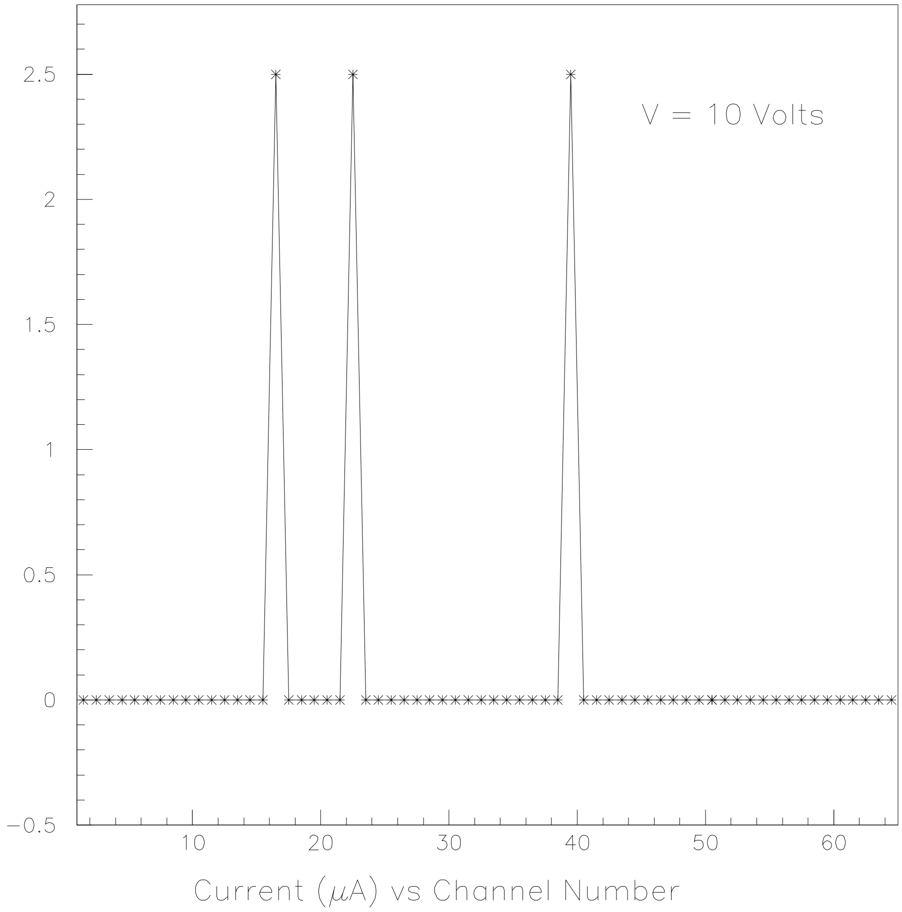


Figure 9: DC current vs. strip number for a CLEO detector wafer.

3.3.3 Shorted wire bonds

To search for shorts between neighboring strips, which can be caused by leaning wire bonds that touch a neighboring bond, we will simply apply a small voltage between neighboring strips and measure the current. The current is limited at the supply to 25 μA. As discussed in Section 3.2, the probe multiplexer allows us to select a strip on one output line and any of the three nearest neighbors on either side of the selected strip on another output line. Shorts are most likely to occur between second nearest neighbors, since the bond pads are staggered. We have verified that we can detect shorted wire bonds using a CLEO detector wafer.

3.4 AC measurements and evaluation with CLEO silicon wafer

The AC measurements are performed with an HP 4284A LCR meter. This instrument can perform capacitance measurements over a frequency range of 20 Hz to 1 MHz, and the test signal amplitude can be varied from 5 mV (rms) to 20 V (rms).

To perform the capacitance measurement in which we search for disconnected or interrupted channels, we connect the LCR meter to the selected strip on one side of the detector wafer (via the probe multiplexer) and to a line from a shorting bar that shorts all of the strips together on the opposite side of the wafer. The shorting bar is made of aluminum, with a piece of copper tape glued on with RTV to provide a softer contact. The shorting is done on the upilex, and it is only necessary that most of the strips be shorted together. The detector is not biased for this measurement, since we we are in effect measuring the coupling capacitance on the unshorted side of the detector. The signal passes through the resistive, unbiased bulk silicon and through the large capacitance of the implants to the shorted strips on the other side. Biasing the detector would introduce a small capacitance in series with the coupling capacitance. One could instead take the signal out through the bias line, but then there would be large resistance in series.

Interrupted lines are also evident in measurements of the interstrip capacitance. Here, one does not need to short the strips on the other side of the detector, but the measurements can be a little more complicated to interpret.

Figure 10 shows the strip capacitance as measured in an unbiased CLEO detector wafer. Several features are evident in the plot: disconnected strips, with a low (parasitic) capacitance due to the upilex, probe, and probe multiplexer; normal strips, with an intermediate capacitance; and pinhole channels, which appear as a much higher capacitance. Note the agreement between the pinhole channels found in this test and those found in the DC test discussed earlier.

If necessary, we can also measure the detector capacitance vs. bias voltage to find the depletion voltage. We would short both sides of the detector at the upilex. For this measurement, it is essential that the bias protection circuit be used (see Fig. 8), since otherwise there would be a risk of damaging the LCR meter. We are in the process of constructing this protection circuit.

3.5 IR pulser measurements and evaluation with CLEO silicon wafer

In many ways, the best test of the detector modules at any stage of assembly after the individual strips have been wire-bonded is to pulse the detector with an infrared LED. We have found that a Seimens SFH450 infrared LED is inexpensive, works extremely well, and can be purchased in a case that allows easy coupling to an optical fiber. The electrical signal to the LED has been controlled in two ways, first by simply driving it with an HP8116A pulser (with a current limiting resistor in series), and second, using an LED driver circuit that we built at UCSB. This circuit, shown in Figure 11, can produce very fast high current pulses of variable width that may be useful when we want to investigate timing issues associated with the hybrid.

The optical system is mounted on a movable xy-stage enclosed in a light-tight box. This is part of the setup that was used for the checkout of the CLEO modules. The stage moves in steps of $\approx 16\mu$m and is presently controlled by a DCX-VM100 VME module from Precision Micro-Control. We have verified that the positioning of this system is reproducible to an accuracy of better than 20 μm. Even though we are able to interface the existing system

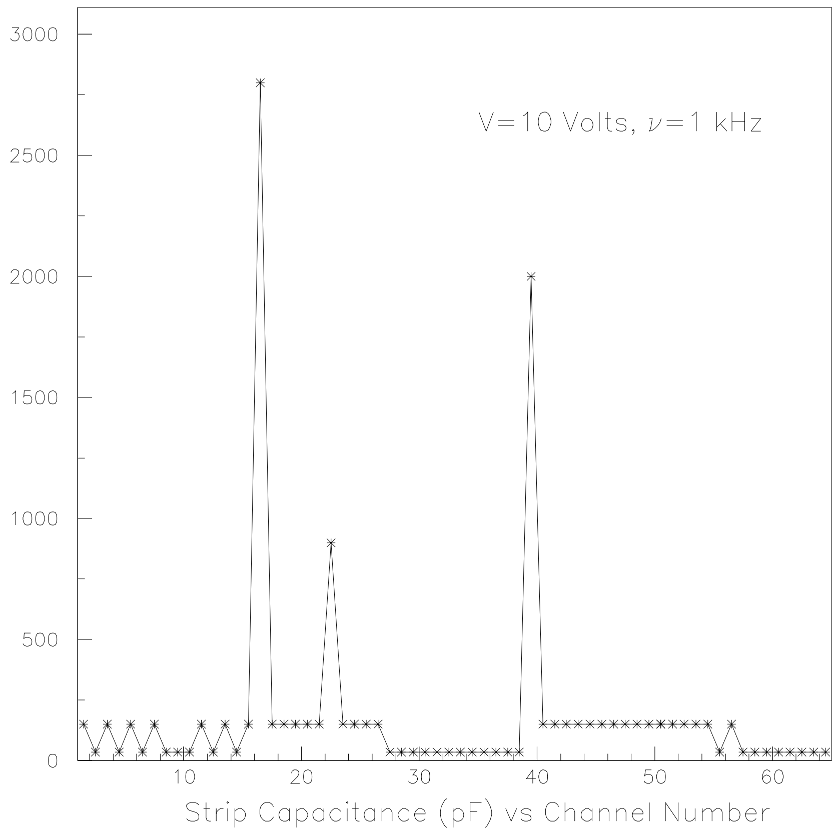


Figure 10: Capacitance vs. strip number for a CLEO detector wafer. Disconnected strips appear as very low values, normal strips as intermediate values, and pinholes as very large values.

to LabView, we think it is simpler to control the stage directly from the PC. The VME controller will be replaced by a PCs-4CX stepping motor controller with encoder input from NuLogic. The encoder will add redundancy to the determination of the position of the light source.

In the pre-hybrid testing phase, we read out the signal from the detector using a LeCroy HQV820-M charge sensitive preamplifier. This preamplifier has a feedback capacitance of $C_f \approx 2$ pF, giving 0.5 mV/fC, or about 2 mV for the signal from a minimum ionizing (min-I) particle. The preamp has a very large feedback resistor, giving a long decay time constant (200 μs), which would be inappropriate for use in the experiment but which is perfectly acceptable in the testing environment. Using the LED pulser and the LeCroy preamp, we are able to observe signals ranging from min-I to over 50 times min-I quite easily. Observation of a sigal at the expected level essentially confirms that the detector strip and its associated readout line are working properly. Given the complexity of the usual methods for reading out silicon detectors via hybrid circuits with custom readout chips, we were somewhat surprised at how easy it is to observe the analog signals from individual strips at the min-I level. Of course, we are reading out only one or two channels at a time, but the signals do have to pass through the probe and the probe multiplexer systems.

One can also verify that the detector is fully depleted by plotting pulse height vs. detector bias voltage; when the detector is fully depleted the pulse height saturates.

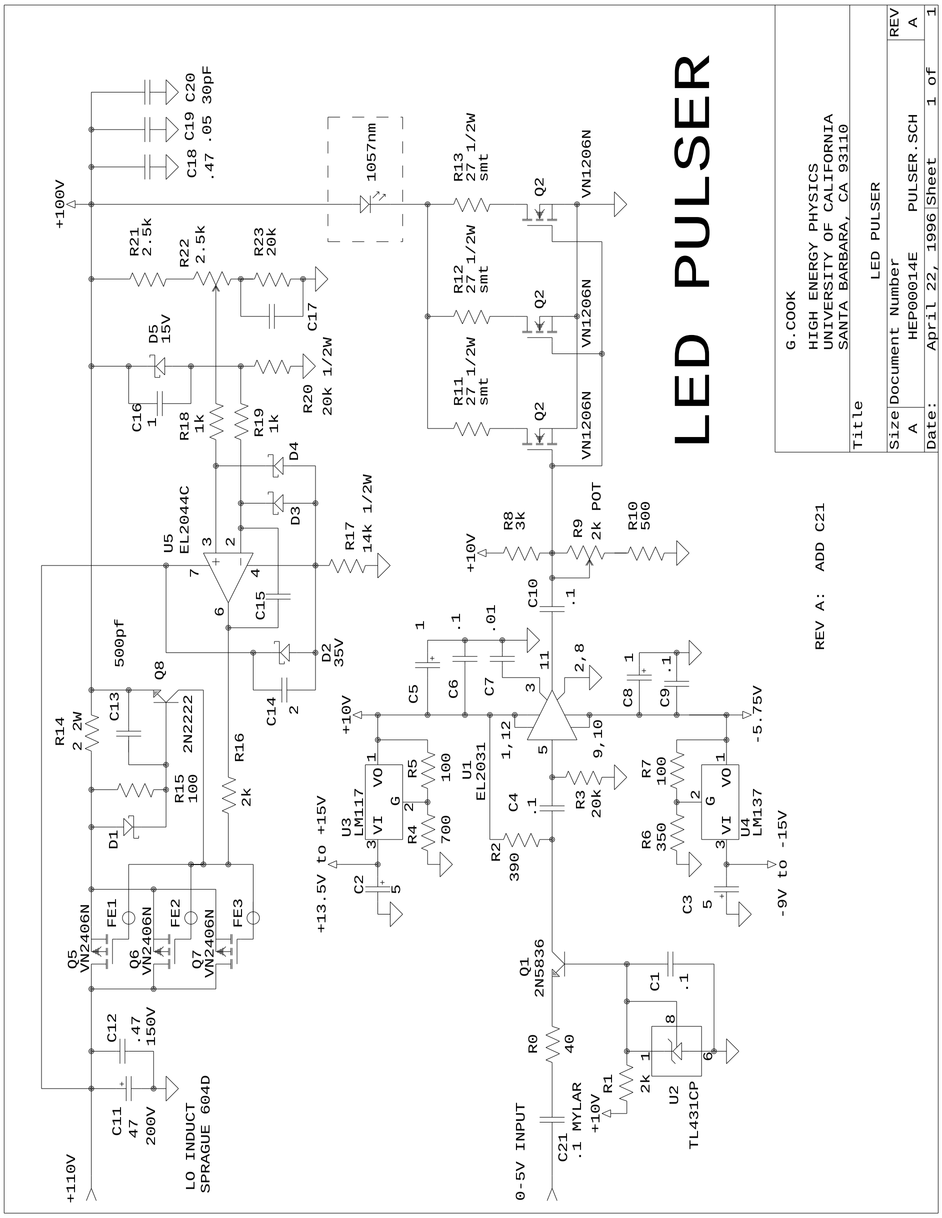


Figure 11: Driver circuit for the infrared LED. This circuit provides high current pulses whose width is controlled by an input control pulse.

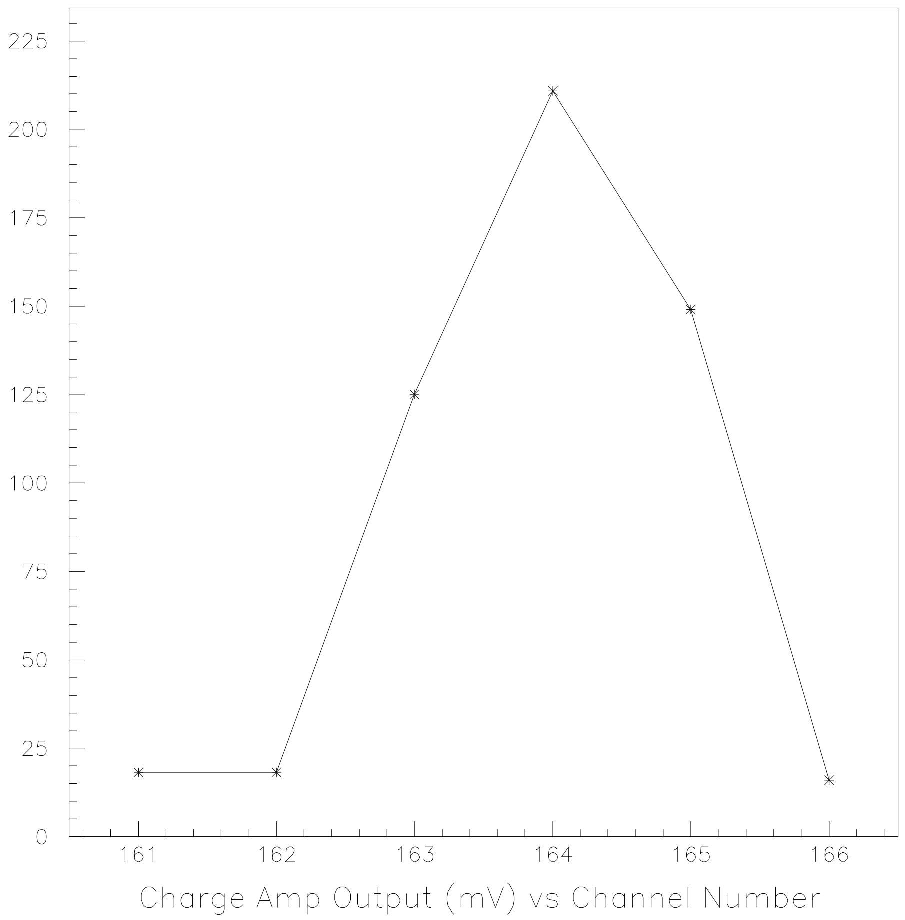


Figure 12: Pulse height vs. channel number for strips illuminated by the LED pulser system. The spot of light covers three strips and can be made smaller if necessary.

4 Sequence of tests prior to hybrid bonding

In this section we list the assembly steps to be performed prior to bonding the hybrids and the electrical tests that will be carried out throughout the process. There is some overlap between the tests to be performed at UCSB and the tests that will be performed in Italy before the DFAs are delivered to us. This overlap is important for the continuity of the assembly process, and it serves to verify that no damage occurred during shipping. We have attempted to design as comprehensive a set of tests as possible that will allow us to detect both forseen and unforseen problems. Experience with the real BaBar detectors will teach us which tests are most useful. Detected problems will be fixed whenever possible. A record of all remaining problems, as well as the charcteristics of each channel/wafer, will be mantained in a database.

The equipment needed to perform these tests is described in detail in section 3. Current and resistance measurements are performed with the Keithley 487 Picoammeter/Voltage Source. Capacitances are measured with the HP4284A LCR meter. All measurements are performed through the probe and probe multiplexer system. The tests can be performed with the detector biased or unbiased. The assembly and testing sequence goes as follows.

- Immediately after receiving the Detector-Fanout-Assemblies (DFAs) from Pisa, and before beginning the bonding process, we will check the integrity of the upilex fanout circuit. At this stage we are only able to check for shorts between upilex traces. This is accomplished by measuring the interstrip resistance. Note that a similar test will have already been performed in Italy as part of a more comprehensive upilex testing procedure. The goal of this test is to verify that no damage occurred to the upilex in shipping.

- Wire-bond the bias and guard ring lines from the upilex to the wafer on both sides.

- Bias the detector and measure the total leakage current versus bias voltage. This measurement will be repeated before each of the testing steps described below.

- Wire-bond the inner row of bonds on the ϕ side to upilex. At this point the full length of the strip is not accessible, since the daisy-chain bonds haven't yet been done.

- Perform the overall test for shorts. This test is accomplished by measuring the resistance between each (bonded) channel and (i) all other channels or (ii) between each (bonded) channel and the ϕ side bias line. Shorts of type (i) can occur if two nearby wire-bonds touch. These can be fixed by combing the bonds. Shorts of type (ii) can be due to pinholes. Since the breakage of the AC capacitor which causes a pinhole is in general dependent on the applied voltage, we will likely perform the resistance measurement at a number of different voltages. The next test to be performed (see below) is a more comprehensive search for pinholes.

- I vs. V pinhole scan for bonded ϕ channels. In this test we measure the current flowing between each AC strip and the corresponding bias line as a function of applied voltage. Note that according to the detector specifications the AC capacitors are supposed to withstand a potential difference of 60 V.

- Interstrip capacitance measurement for bonded ϕ strips. Measure capacitance between each bonded strip and its nearest or second nearest neighbor. Disconnected bonds will result in abnormally low values of interstrip capacitance.

- Interstrip resistance. Measure resistance between each bonded strip and its nearest or second nearest neighbor. The goal of this test is to find shorts between nearby channels. This measurement is redundant with the overall test for shorts described above, however it will be useful in pinpointing the location of any such short.

- Bond outer row of bonds (over the top) on the ϕ side to upilex.

- Repeat battery of tests on ϕ side : (i) overall test for shorts, (ii) IV pinhole scan, (iii) interstrip capacitance, (iv) interstrip resistance.

- Bond daisy chain bonds between different silicon wafers in the same DFA, ϕ side.

- Repeat battery of tests on ϕ side : (i) overall test for shorts, (ii) IV pinholew scan, (iii) interstrip capacitance, (iv) interstrip resistance.

- LED scan, ϕ side. Using the XY stage and the IR LED, we will scan the LED light over the whole detector. The channel corresponding to the position of the LED light will be connected to the charge amplifier through the scanner. The output of the charge amplifier will be read-out through an analog-to-digital-converter. This test will be useful in verifying the integrity of the silicon wafers and will also detect disconnected wire-bonds.

- Bond all channels on z side.

- Perform battery of tests on z-side : (i) overall test for shorts, (ii) IV pinhole scan, (iii) interstrip capacitance, (iv) interstrip resistance. Repeat battery of tests on ϕ side to insure that handling of detector did not introduce additional damages on the ϕ side.

- Measure bulk capacitance as a function of bias voltage. This is accomplished by shorting all AC strips on each side together using the shorting bar described in section 3.2 and measuring the capacitance between the two sides. This measurements verifies the value of the depletion voltage.

- measure capacitance between each strip (on both sides) and all other strips, shorted together, on the opposite side. This measurement is sensitive to broken wire bonds.

- LED scan, both sides.

5 Description and sequence of tests after bonding to hybrid

In this Section we describe the series of tests to be performed with the detectors bonded to the hybrids. Before committing to bonding a given hybrid to a DFA, we will repeat the set of tests on the hybrid performed in Milan, to make sure that the hybrid was not damaged in shipping. We will first verify the integrity of the communication between the DAQ board and the hybrid, and we will then perform threshold and charge injection scans.

Members of the UCSB group are collaborating with the LBL BaBar Data Acquisition group (Mike Levi and Armin Karcher) to prepare the necessary software to communicate with the hybrid through a standard BaBar DAQ readout module, the SVT personality module, and the SVT transition card. The BaBar DAQ module is a VME card that is controlled by an embedded VME processor, such as a Motorola MVME1604 or MVME167, running the VxWorks operating system. For the purposes of testing, we have decided to control the VME processor from a remote Unix workstation through a transparent RPC bridge based on software developed for CDF silicon detector test stands [1]. The user interacts with this package through an easy to use graphical interface based on Tcl-Tk, see Figure 13. Immediate feed-back is provided by on-line histograms generated using the HistScope package [2]. The data can also be written out to a file for offline analysis.

Once the hybrids are bonded to the DFAs, we will repeat the measurement of leakage current as a function of bias voltage to verify that the detectors were not damaged in the wire bonding process and that the bias bonds are in place. We will then again perform the same hybrid tests (communication, theshold and charge injection scans) that had been performed on the bare hybrids prior to wire bonding. We will then perform an LED scan of the DFAs, reading out the detectors through the standard BaBar readout chain. We envision that in this testing phase we will make use of a prototype BaBar-SVT power supply system.

The LED scans with the hybrids bonded will be performed on a similar stage as the one used for the earlier scans with readout through the LeCroy charge preamplifier and LabView. We will however use a separate setup, since the schedule of the SVT construction is such that we will be performing some of these tests in parallel. Since the hybrid readout system is VME based, we will be also controlling the xy stage through VME, e.g. using the DCX-VM100 VME module from Precision Micro-Control.

The LED scans with the attched hybrids will result in a detailed map of the response of each individual channel with its associated electronics. The intensity of the LED light will be varied to study the time-over-threshold response as a function of energy deposition in the silicon wafers. In order to check for shorted wire bonds, the LED light will also need to be somewhat more tightly focussed than in the present system. Once again, results from these tests will be stored in a database.

After the LED scan, we will glue the ribs to the DFAs, and assemble the forward and backward DFAs into a module. At this point, we will repeat the hybrid tests and possibly the LED scan.

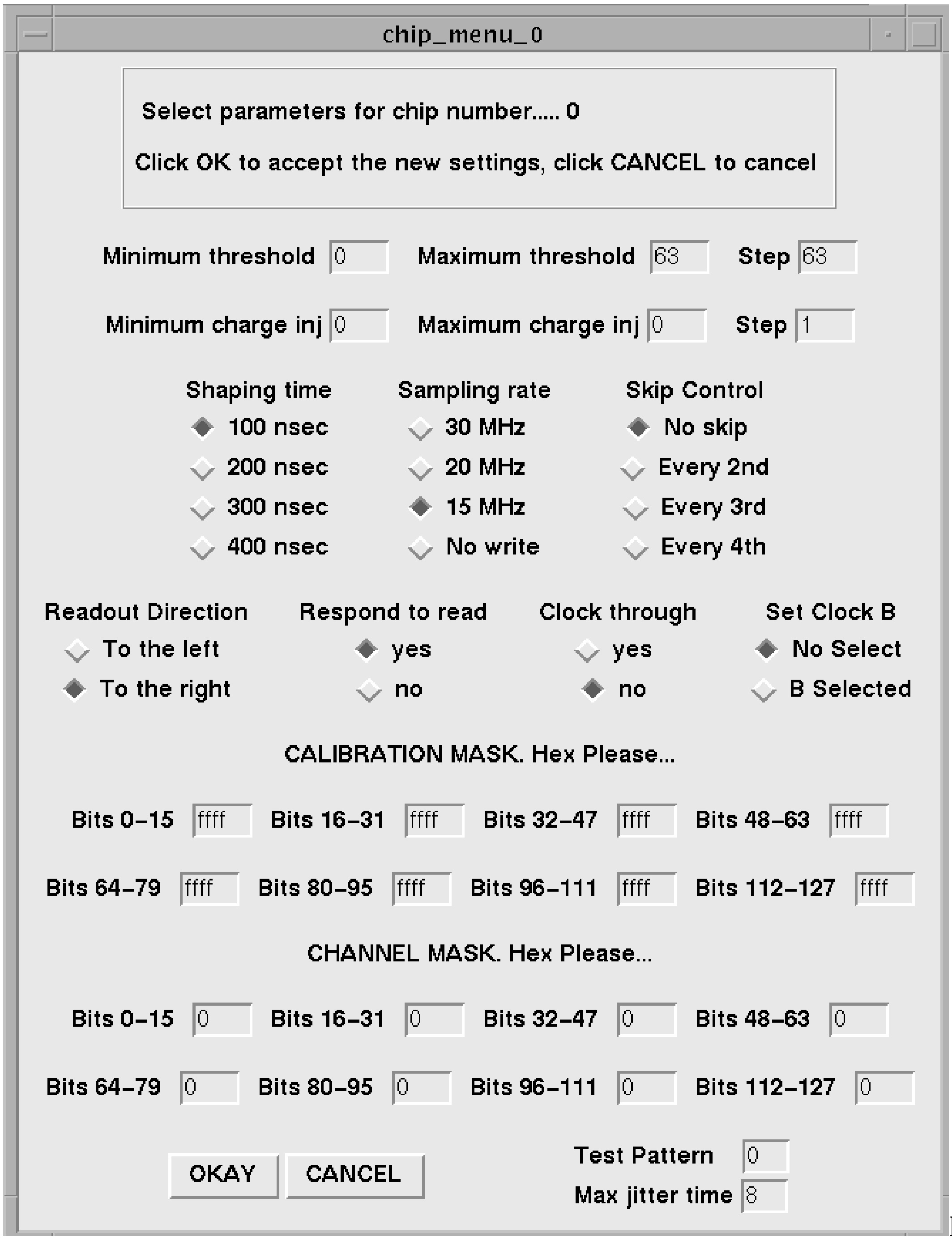


Figure 13: The Tcl-Tk menu used to control the parameters of the front end chips for threshold scans and/or charge injection runs.

6 Conclusions

We have designed and evaluated a set of tests that will allow us to maintain good quality control during the SVT module assembly process. All of our tests were studied with a CLEO silicon wafer and are effective in finding the types of problems that are likely to occur. The tests are sufficiently broad that unforseen problems that can significantly affect the detector operation should be evident. The overlap among the tests should help us to diagnose the nature of any new problems.

Although most of the instrumentation has now been tested using CLEO wafers, some of it is still in the prototype stage. The prototype multipin probe for making electrical contact with the upilex works very well, and a production version is now underway. Nearly all of the electronics has been designed and much of it tested during our evaluations using the CLEO detectors. Significant work remains on upgrading the xy stages, on writing data acquisition software and database management tools, and in completing the mechanics of the two production test stands. We expect to be ready for the beginning of module assembly in mid-summer 1996.

References

[1] E. Gottlieb, T. Thomas, and M. Gold, CDF Note No. 3082.

[2] Histo-Scope V3.1 User's Guide, Fermilab Physics Analysis Tools Group, SP0034.